



Basic Information:

Title:	Advance Computer Architecture	Code:	IT 665
Program:	MBIT (Major in Information Technology)	Credit Hours:	Three (03)
Sessions:	30 Classes + Mid Term + Final Term	Pre-Requisite:	BBIT (Major in IT)

Course Description:

The course of computer architecture is concerned with the structure and behavior of the various functional modules of computer and how they interact to provide the processing needs of the user. Computer design is concerned with the development of hardware for the computer taking into consideration a given set of specifications. Detailed steps that a computer designer must go through in the organization and architecture of CPU are also covered

Learning Outcomes:

After the completion of this course, it is expected that students who will involve themselves in the knowledge base working of the course will be capable to

- an ability to understand the design of a pipelined CPU and cache hierarchy*
- an ability to analyze and evaluate CPU and memory hierarchy performance*
- an understanding of trade-offs in modern CPU design including issues affecting superscalar and dynamically scheduled architectures*
- an understanding of hardware design of multiprocessors including cache coherence and synchronization*
- an ability to understand the advanced domain specific architectures.*

Teaching Learning Methodology:

The formal teaching component of this course consists of active student participation in and contribution to all forms of teaching and learning i.e. lectures, discussions, research assignments and projects. Lectures will be twice a week of 90 min each.

Group Configurations:

One of the objectives of this course is to encourage and facilitate teamwork. Class will have to make a group of four for projects and research assignments. It is recommended that student will form their own groups. As a general guideline, your group should have members with diverse skill sets including people who are proficient or have aptitude for different subject areas.

Weekly Term Plan

Wk	Lecture Topic
01	<i>Course Introduction and Quantifying Cost and performance</i>
02	<i>Instruction Set Architecture</i>
03	<i>Register Reference Instructions, Verilog I</i>
04	<i>MIPS Architecture</i>
05	<i>Data Path design of MIPS Instructions, Verilog II</i>
06	<i>Pipelining of MIPS</i>
07	<i>Handling Pipeline Hazards</i>
08	<i>Memory Hierarchies and Performance,</i>
09	<i>Mid Term Examinations</i>
10	<i>Single Cycle and Multi Cycle Implementation of MIPS</i>
11	<i>Multicore, Multiprocessor and Clusters Architecture</i>
12	<i>New Era of Architecture: Domain specific architecture (DSA)</i>
13	<i>GPUs Architecture</i>
14	<i>NVIDIA Architecture</i>
15	<i>AMD Architecture</i>
16	<i>Final Term Examination</i>



Topics in Detail

Quantifying cost and performance

Performance

Power Wall

Computer Organization

8086 architecture

Memory addressing

Memory segments

MIPS

Logical Instructions

Instructions for making decision

MIPS addressing for 32-bit immediate and Addresses

ARM Instructions

X86 Instructions

Processor Design

Logic Design Conventions

Building a Datapath

An overview of Pipelining

Pipelined Datapath and control

Data Hazards

Control Hazards

Exceptions

Parallelism and Advanced Instructions level parallelism

Memory Hierarchy

Cache basic

Measuring and Improving cache performance

Virtual memory and Virtual machines

Cache coherence

Cache controllers

Multicore, Multiprocessor and Clusters Architecture

The difficulty of creating parallel programs

Shared Memory Multiprocessors

Hardware Multithreading

Multiprocessors Network Topologies

Multiprocessors Benchmarking

Four Multicores using Roofline Model

Domain Specific Architecture

NVIDIA Architecture

AMD Architecture

Verilog

Text & Recommended Readings	Assignment Specification
1. <i>Computer Organization and Design by Hennessy and Patterson</i>	<i>Microsoft Word for Documentation</i>
2. <i>Computer System Architecture by Morris Mano</i>	<i>Headings</i> <i>Arial 11pt Bold</i>
	<i>Normal Text</i> <i>Times New Roman 10pt</i>
	<i>Header Footer</i> <i>Times New Roman 8pt</i>
	<i>Paragraph</i> <i>Single Line Spacing</i>
	<i>First Line Indent 1.0 cm</i>
	<i>Page Margins</i> <i>2 cm from each side</i>



Grading Policy:

Final Grade for this course will be the cumulated result of the following term work with relevant participation according to the quoted percentage.

Sessional	25%		Mid Term	35%		Final Term	40%
Assignments	10 %		Mid Term Exam	25%		Final Exam	30%
Quizzes	10%		Major Report/Work	10%		Case Study/ Project/ Term Paper	10%
Presentations	05%						

Remember subdivision of Mid Term and Final Term Examination should be done only in extreme cases of very essential and major Grading Instruments.

Dishonest Practices & Plagiarism

Any student found responsible for dishonest practice/cheating (e.g. copying the work of others, use of unauthorized material in Grading Instruments) in relation to any piece of Grading Instrument will face penalties like deduction of marks, grade 'F' in the course, or in extreme cases, suspension and rustication from IBIT.

For details consult Plagiarism Policy of PU at <http://pu.edu.pk/dpcc/downloads/Plagiarism-Policy.pdf>

Grading System:

Letter Grade	Grade Point	Num Equivalence
A	4.00	85 – 100 %
A-	3.70	80 – 84 %
B+	3.30	75 – 79%
B	3.00	70 – 74 %
B-	2.70	65 – 69 %
C+	2.30	61 – 64 %
C	2.00	58 – 60 %
C-	1.70	55 – 57 %
D	1.00	50 – 54 %
F	0.00	Below 50 %
I	Incomplete	*
W	Withdraw	*

Norms to Course:

- ✓ Submission Date and Time for the term instruments is always **Un-Extendable**.
- ✓ 7 Absentees in class will be result in forced withdrawal. **(PU Policy)**
- ✓ Re-sit in Mid and Final Term will cause you a loss of 2 and 3 grade marks respectively. **(PU Policy)**
- ✓ This is your responsibility to keep track of your position in class evaluation units.
- ✓ After the submission date, NO excuse will be entertained.
- ✓ **Keep a copy of all submitted Grading Instruments.**
- ✓ Assignment is acceptable only in its Entirety.
- ✓ No make up for any assignment and quiz.
- ✓ Copied & Shared work will score Zero.
- ✓ Assignments are Individual.

Good Luck