Spring Term

Basic Information:

Title:	Digital Logic Design	**Code**	IT-162
Program:	BBIT	**Credit Hours:**	Three (03)
Sessions:	30 Classes + Mid Term + Final Term	**Pre-Requisite:**	IT 160

Course Description:

This course covers the design of integrated circuits for the digital systems. Emphasis is placed on theoretical concepts and systematic techniques of synthesis which can be applied to realistic digital systems design.

Learning Outcomes:

After the completion of this course, it is expected that students who will involve themselves in the knowledge base working of the course will be capable to

1. *Design logic level models, including Boolean algebra, Arithmetic Circuits, State Machines and ALU.*
2. *Design sequential circuits, including latches, flip-flops, registers and counters.*
3. *Understand the role of time, frequency and interrupts in digital computers.*
4. *Understand memory, including flip flops, RAM and ROM.*
5. *Understand and design of control, data and address bus along with their communication with ALU, memory and I/O devices.*

Teaching Learning Methodology:

The formal teaching component of this course consists of active student participation in and contribution to all forms of teaching and learning i.e. lectures, discussions, research assignments and projects. Lectures will be twice a week of 90 min each.

Group Configurations:

One of the objectives of this course is to encourage and facilitate teamwork. Class will have to make a group of <u>two</u> for projects and research assignments. It is recommended that student will form their own groups. As a general guideline, your group should have members with diverse skill sets including people who are proficient or have aptitude for different subject areas.

Weekly Term Plan

Wk	Lecture Topic	Sessional Activities
01	*Digital Systems and Digital Numbers*	
02	*Boolean Algebra and Circuit Design*	*Assignment 1 (a)*
03	*Standard and Canonical Forms*	*Quiz 1*
04	*Gate-level Minimization, MSI Logic Circuits*	*Assignment 1 (b)*
05	*Sequential Circuits*	*Quiz 2*
06	*Registers*	*Assignment 2 (Verilog HDL)*
07	*ALU Design*	*Assignment 3 ((a & b) (Design + VHDL)*
08	*Mid Term Examination*	
09	*Synthesizable HDL Models of Sequential Circuits*	
10	*Counters*	*Term Project Proposal*
11	*RAM Architecture, RAM Read/Write Operations*	*Quiz 3*
12	*ROM Architecture, ROM Operations*	*Term Project Deliverable 1*
13	*Register Transfer Level (RTL), RTL in HDL*	*Assignment 4 + Term Project Deliverable 2*
14	*Algorithmic State Machines (ASM)*	*Quiz 4* *Term Project Final Evaluation*
15	*Synchronizing Data Bus, Control Bus and Address Bus operations with ALU and Memory*	*Finalizing Sessional Activities*
16	*Final Term Examination*	

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Topics in Detail

Digital Systems and Binary Numbers
- *Number Systems and Conversions*
- *Complements*

Describing Logic Circuits
- *Basic Logic Gates*
- *Boolean Theorems*
- *Boolean Algebra*
  - *Boolean Functions*
  - *Circuits design for Boolean functions*
  - *Simplification of Boolean functions using Boolean Theorems*
- *Introduction to Verilog HDL*

Gate-level Minimization
- *Standard and Canonical forms*
  - *Sum of products and sum of minterms*
  - *Product of sums and product of maxterms*
- *Simplification of Boolean Expressions using K-Map*
- *NAND and NOR implementations*

MSI Logic Circuits
- *Decoders*
- *Encoders*
- *Data Selectors*
- *Data Distributors*

Synchronous Sequential Circuits
- *Sequential Circuits*
- *Latches and Flip flops*
- *Analysis of clocked sequential circuits*

Registers
- *Data Storage and Transfer: Registers*
- *Serial Data Transfer: Shift Registers*

Arithmetic Logic Unit Design
- *Arithmetic Circuits*
- *Analysis and Design procedures of Combinational Circuits*
  - *Binary Adder-Subtractor*
  - *Binary Multiplier*
  - *Magnitude Comparator*
  - *Arithmetic Logic Unit*
- *ALU integrated Circuits*

Synthesizable HDL Models of Sequential Circuits

Counters
  - *Ripple counters*
  - *Parallel Counters*
- *HDL for Registers and Counters*

Memory Unit
- *Random Access Memory (RAM) Architecture*
- *RAM Read/Write Operations*
- *Memory Decoding*
- *Read-only Memory*
- *Register Transfer Level (RTL) in HDL*

Algorithmic State Machines (ASM)
  - *Mealy FSM*
  - *Moore FSM*

Synchronizing Data Bus, Control Bus and Address Bus operations with ALU and Memory

Text & Recommended Readings

1. *Digital Design 4th Edition*
   by Morris Mano
   Digital Systems: Principles and Applications
   by Ronald J. Tocci
   10th Edition
2. *Fundamentals of Digital Logic with VHDL design 3rd Edition*
   by Stephen Brown

Assignment Specification

1. *Microsoft Word for Documentation*
   Headings Arial 11pt Bold
   Normal Text Times New Roman 10pt
   Header Footer Times New Roman 8pt
   Paragraph Single Line Spacing
   First Line Indent 1.0 cm
   Page Margins 2 cm from each side
2. *Program Files for VHDL in .zip folder*

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Grading Policy:

Final Grade for this course will be the cumulated result of the following term work with relevant participation according to the quoted percentage.

Sessional	**25%**		***Mid Term***	**35%**		***Final Term***	**40%**
Assignments	10 %		*Mid Term Exam*	25%		*Final Exam*	30%
Quizzes	10%		*Major Report/Work*	10%		*Case Study/ Project/ Term Paper*	10%
Presentations	05%						

Remember subdivision of Mid Term and Final Term Examination should be done only in extreme cases of very essential and major Grading Instruments.

Dishonest Practices & Plagiarism

Any student found responsible for dishonest practice/cheating (e.g. copying the work of others, use of unauthorized material in Grading Instruments) in relation to any piece of Grading Instrument will face penalties like deduction of marks, grade 'F' in the course, or in extreme cases, suspension and rustication from IBIT.

For details consult PU Plagiarism Policy at http://pu.edu.pk/dpcc/downloads/Plagiarism-Policy.pdf

Grading System:

Letter Grade	Grade Point	Num Equivalence
A	4.00	85 – 100 %
A-	3.70	80 – 84 %
B+	3.30	75 – 79%
B	3.00	70 – 74 %
B-	2.70	65 – 69 %
C+	2.30	61 – 64 %
C	2.00	58 – 60 %
C-	1.70	55 – 57 %
D	1.00	50 – 54 %
F	0.00	Below 50 %
I	Incomplete	*
W	Withdraw	*

Norms to Course:

- ✓ *Submission Date and Time for the term instruments is always* **Un-Extendable**.
- ✓ *5 Absentees in class will result in forced withdrawal.* ***(PU Policy)***
- ✓ *Re-sit in Mid and Final Term will cause you a loss of 2 and 3 grade marks respectively.* ***(PU Policy)***
- ✓ *This is your responsibility to keep track of your position in class evaluation units.*
- ✓ *After the submission date, NO excuse will be entertained.*
- ✓ ***Keep a copy of all submitted Grading Instruments.***
- ✓ *Assignment is acceptable only in its Entirety.*
- ✓ *No make up for any assignment and quiz.*
- ✓ *Copied & Shared work will score Zero.*
- ✓ *Assignments are Individual.*

Good Luck

For the Spring Term